2831

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Per-Erik Nordal et al. Attorney Docket No.: P67191US0

Serial No.: 09/926,531 Group Art Unit: 2831

Filed: November 15, 2001 Examiner: Hung V. NGO

For: VERTICAL ELECTRICAL INTERCONNECTIONS IN A STACK

TRANSMITTAL

BOX- PATENT NON-FEE AMENDMENT
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Transmitted herewith is a Response in the above captioned application.

_____Small Entity status of this application under 37 C.F.R. 1.9 and 1.27 has been established by a verified statement previously submitted.

____A verified Statement to establish small entity status under 37 C.F.R. 1.9 and 1.27 is enclosed.

_____No additional fee is required.

The fee has been calculated as shown below:

Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Small Entity Rate Addit. Fee (or)	Other Than A Small Entity Rate Addit. Fee
Total -	20 =	0	x09 = $	x 18 = $
Indep. -	3 =	0	x42 = $	x 84 = $
First Presentation of Multiple Dependent Claim			x140= $	+280 = $
Total Additional Fee			$	$

____ A check in the amount of $_____ is attached for:

__XX__ If a Petition for Extension of Time is necessary and the Petition and/or the check is not enclosed, this will act as the Petition and applicant herewith petitions the Commissioner to extend the time for response and charge any fees necessary under 37 CFR 1.17 (a)(1)-(5) to Deposit Account No. 06-1358. The Commissioner is also authorized to charge payment of any other additional fees associated with this communication or credit any overpayment to Deposit Account No. 06-1358. A duplicate copy of this sheet is attached.

JACOBSON HOLMAN, PLLC

Dated: December 20, 2002
400 Seventh Street, N. W.
Washington, D.C. 20004-2201 By: Jonathan L. Scherer
JLS/dmt Reg. No. 29,851

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#8 Response D. Evans 1.6.03

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Per-Erik Nordal et al. Attorney Docket No.: P67191US0

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For: VERTICAL ELECTRICAL INTERCONNECTIONS IN A STACK

RESPONSE

BOX NON-FEE AMENDMENT.
Commissioner for Patents
Washington, D.C. 20231

Sir:

The Examiner has rejected the claims in the Office Action of October 3, 2002 (paper No. 6) as anticipated by respectively U.S. 6,215,182 (Ozawa et al.) and U.S. 6,376,904 (Haba et al.) Both these publications are directed towards a wholly different technology, viz. the interconnection of integrated circuit "dies" provided in a stacked arrangement.

In contrast to the present invention Ozawa et al. moreover completely relies on wire bonding techniques, which is not the case of the present invention and as far as it can be seen the same is the case for Haba et al., particularly in the case of the cited fig. 3a disclosing the bonding wires 440a-440j. In both cases of Ozawa et al and Haba et al the bonding wires which according to Haba et al form multidrop transmission lines, connect the integrated circuit dies with connectors on a so-called BGA-

substrate, that is a semiconductor device of the ball grid array type.

In the present invention, however layered structures wherein each layer may comprise sublayers, e.g. electrode layers, and essentially all are realized in a thin-film technology. The layers are connected to an underlying substrate by means of staggered vias deposited on the surface of each layer or alternatively each sublayer. The vias are carried over the edge of each layer as a continuous deposited structure in order to provide contact between the stacked and staggered layers and a substrate which may be optional.

In case the present invention is realized or embodied in a thin-film memory device, it will be necessary to connect each layered memory device with active circuitry for driving and control. Whereas such active circuitry may be provided in each device in separate and adjoining sublayers thereof, they presently are provided in the form of integrated circuitry provided in the substrate and realized in CMOS technology.

The possibility of creating conducting parts and connecting structures according to the invention as being deposited on the surface of each layer device and on and over the steps of staggered structure, depends on the fact that each layer and device is formed in the submicron range and hence it will be possible to negotiate the vertical edge of he steps due to the step height at

most lying in the low micrometer or even submicrometer range. As Ozawa et al. and Haba et al both are concerned with interconnecting stacked integrated circuit dies, it is evident that the height of the dyes will be in the millimeter range, see e.g. fig. 3c of Haba where it is indicated that the step height is 0.5 mm. It will be impossible to negotiate a step height of this dimension by applying the inventive technology and that is precisely why all prior art actually relies on wire bond or related technologies for obtaining interconnection in stacked integrated circuit structures. An alternative is of course as disclosed by Haba et al. to use a flexible substrate material with deposited conducting parts, see e.g. fig. 7b-7d of Haba et al. In any case the prior art interconnections in the stack are not formed as deposited structures on the surfaces of layers and sublayers, but rather as discrete and separate elements.

Ozawa et al was filed in the U.S. on March 20, 2000 and Haba et al on October 10, 2000, both dates being after the filing date of March 15, 2000, for the Norwegian priority application. Haba et al was filed as a continuation-in-part application on October 10, 2000, based upon an application filed December 23, 1999. Therefore, if the subject matter of the claims of the Haba et al patent were based upon the subject matter filed October 10, 2000, Haba et al is <u>not</u> prior art. However, it is not necessary, to overcome the effective date of Haba (or even Ogawa), as it is

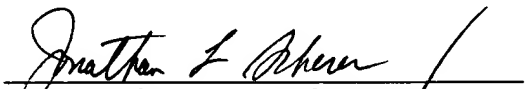
evident from the above comments that on the merits neither Ozawa et al nor Haba et al can be regarded as anticipatory prior art.

Based on the foregoing remarks, it is respectfully submitted that the claims in the present application, as they now stand, patentably distinguish over the references cited and applied by the Examiner and are, therefore, in condition for allowance. A Notice of Allowance is in order, and such favorable action and reconsideration are respectfully requested.

However, if after reviewing the above remarks, the Examiner has any questions or comments, he is cordially invited to contact the undersigned attorneys.

Respectfully submitted,

JACOBSON HOLMAN, PLLC

By: 
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Date: December 20, 2002
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